Design and Implementation of MIMO-OFDM using Encoding and Decoding techniques on FPGA

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Abstract— In this paper, we present a memory-efficient and faster convolution encoding and adaptive viterbi decoding implementation technique for MIMO-OFDM communication systems on FPGA. A method for the 1/3 convloution encoder and Modified viterbi decoder design used for coding techniques on FPGA. Our design utilizes the minimum required on-chip memory for the MIMO-OFDM implementation. Using the proposed design method, the I/O rate for MIMO-OFDM based communication systems are doubled for 2×2 MIMO systems. The whole design is implemented using Xilinx ISE 13.4 using VERILOG on Vitrex 5 FPGA and simulated using Modelsim 6.3f.

Index Terms— MIMO, 802.16, OFDM, FPGA.

1 INTRODUCTION

The IEEE 802.16 defines the standard for broadband wireless access covering the physical layer and medium access specifications for wireless metropolitan area networks (WMAN). The IEEE 802.16 Air Interface Standard is a technology that is playing a key role in fixed broadband wireless MAN [1]. The FEC system in the standard plays a very important role in its performance. A number of techniques are being used to achieve highly effective error-control coding such as Turbo codes and concatenated codes. Memory utilization and frequent memory accesses time are a crucial part of interleaver design, targeting less memory utilization and reduced memory access in order to reduce the power dissipation of the overall system.

A memory-efficient interleaver design method has been proposed in [2], where the author presents divided memory bank architecture for the implementation of interleaver for IEEE 802.16e. An efficient memory memory address manipulation technique that can improve the performance interleaver is proposed in [3], but no details are provided. An analysis of the effects of interleaving process on spectral efficiency of IEEE 802.16 for different environments is done in [4]. They also measured the system throughput and interleaver block delay, and proposed solutions for interleaver design.

OFDM has been adopted as the modulation method of choice for practically all the new wireless technologies being used and developed today. It is perhaps the most spectrally efficient method discovered so far, and it mitigates the severe problem of multipath propagation that causes massive data errors and loss of signal in the microwave and UHF spectrum. Motive of doing this project is to improve the performance of the encoding and decoding techniques in terms of speed and area in OFDM communication system.

The selection of efficient encoding and decoding techniques and interleaver is a critical issue in an communication channel. The simplest type of interleaver merely permutes all lines of the input bit stream randomly. The effect of this random shuffling makes almost all symbols correlated with each other. It rearranges the elements of its input vector using a random permutation. In this method of interleaving the memory space used by the buffer is very large this in turn makes the speed of the interleaver block to be less.

The main aim is design and development of convolution encoder and modified viterbi decoder in MIMO OFDM System and study the simulation of modulation scheme (16-QAM) deployed over OFDM using convolutional code rate 1/3 with interleaver (Matrix) which is an important part in the design of a communication system using MIMO-OFDM technique which will be optimized in terms of Area and Speed.

The paper is organized as follows. Section 2 gives a Brief review of the MIMO and previous OFDM techniques. Section 3 presents the Implementation of MIMO-OFDM Technique in detail which includes induvial modules of both transmitter and receiver design. Section 4 presents the simulation results and anlaysis of MIMO-OFM. A conclusion is given in Section 5.

2 RELATED WORK

Taewon Hwang et al [6] have described briefly about OFDM

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for wireless communications, starting with the basic principle of OFDM and techniques to deal with impairments in wireless systems, including channel estimation, timing and frequency-offset estimation, ICI mitigation, and PAPR reductionand introduced related modulation and access schemes, such as OFDM, SC-FDE, EST-based modulation, MC-CDMA, and OFDMA. They have summarized the MIMO techniques for OFDM and the wireless applications of OFDM.

Fernando H. Gregorio [7]have presented coding and interleaving techniques and their performance was evaluated in a WLAN environment. This work showed the importance of coding and interleaving techniques to improve the quality of service in a IEEE802.11 service. It is possible that other techniques, as Turbo Coding, Trellis Modulation and Concatenated codes, can bein- corporated in future WLAN standards but it is necessary to evaluate the improvement and the increment in the complexity that their incorporation produces.

M.A. Mohamed ae all [8] developed a base band OFDM transmitter and receiver using VHDL codes and e implemented using FPGA. The output from each module was tested using appropriate software to ensure the correctness of the output result. On the transmitter part there are four blocks which consists of mapper (modulation), serial to parallel, IFFT and parallel to serial block. Each of these blocks were tested using FPGA. During the implementation stage; the same process was done at the receiver part whereby each of the modules was tested during design process. The relation between SNR and BER for different systems for OFDM were introduced using Matlab software tools.

Jeff Foerster et al [9] have presented a s contribution to provide the performance of the concatenated Reed-Solomon and convolutional code that is described in Mode A of the current draft physical layer standard. The code provided was only applicable for the downstream channel that uses a continuous transmission stream in a frequency division duplexed (FDD) system. As a result, it was not appropriate for a frequency switched division duplexed (FSDD) system or a time division duplexed (TDD) system, unless the interleaver is shortened and the convolutional code is terminated through tail biting.In addition, it was not appropriate for systems that employ adaptive modulation in the downstream channel, due to the overall length of the concatenated code and interleaver. However, the code provided had a strong coding gain with flexibility in the selection of the code rate and modulation level

Bijoy Kumar Upadhyaya et al [10] presented a full FPGA implementation of WiMAX multimode interleaver. It proposes a novel finite state machine based address generator used for generation of write and read addresses for the interleaver memory. The interleaver memory is implemented using dual port Block RAM of Xilinx Spartan-3 FPGA. The presented circuit supports all the code rates and modulation schemes permitted under IEEE 802.16e standard. The simulation results endorse the correct operation of both address generator and interleaver as a whole. The novelty of the approach includes higher operating frequency and better resource utilization in FPGA.

Mai Abdelhakim [11] have proposed a novel adaptive puncturing scheme for varying the code rate within a single codeword in coded OFDMA systems. The proposed structure enables to use longer codewords independent of the tile size. Different rates, used to load the tiles, are obtained through puncturing the long codeword differently on each tile. We have also proposed two interleaving methods, a puncturing dependant interleaver (PDI) and interleaved puncturing (IntP). In the PDI method the size of the interleavers depends on the number of tiles that are loaded with the same rate. The IntP method uses a larger interleaver independent of the code rates used to load the different tiles. We show the performance results obtained by using adaptive puncturing along with AMC. The new adaptive puncturing scheme is evaluated in case of constantand variable bit rates.

Michael Francis et al [12] has provided an overall view of the digital television broadcast standards and has outlined how Xilinx helps to meet the FEC requirements, in particular, and DSP requirement, in general, by offering a fully flexible and reprogrammable way of implementing standard blocks with changeable parameters. In certain cases, some of the hard work has already been done––a drop down menu in the Xilinx core generating software allows selection of the DVB or the ATSC option. Alternatively, the intuitive GUI allows the users to specify their own values to support other broadcast standards. Furthermore, the FEC may be replaced by improved algorithms in next generation specifications.

3 MIMO-OFDM IMPLEMENTATION

MIMO- transmitter block diagram is shown in Figure.1. A user provides input binary data. The Convolution Encoder block encodes the data with code rate 1/3. It produces one binary stream for each of the three convolutional codes and multiplexes them into a single stream. As a result, it changes the rate to twice the number of bits per second with respect to its input. The Interleaver block performs Forney interleaving and produces a binary stream of interleaved data.

The 16-Quadrature amplitude modulation is a combination of ASK and PSK so that a maximum contrast between each signal unit and so on is achieved and produces real and imaginary signals. The symbol generator increases the number of bits by replicating the modulated output and produces the results. The zero padding block pads the same number of zeros to the LSB and MSB of the symbol generator output and produces the results. The Inverse Fast Fourier Transform block converts IFFT inputs into N parallel streams, maps them onto orthogonal carriers, converts the N parallel output streams into a serial stream and produces the OFDM signal. The main result of cyclic prefix is that the Intersymbol Interference (ISI) and Intercarrier Interference (ICI) may be spectrally concentrated.

At the receiver, inverse operation of transmitter is done. The output was transformed back to the in-phase and quadrature components by the FFT block. The demodulator block demaps them into symbols then converts them into a serial bit stream.

The Deinterleaver block produces results and is provided as input to the Viterbi Decoder that recovers the binary data that should be the same as user data.

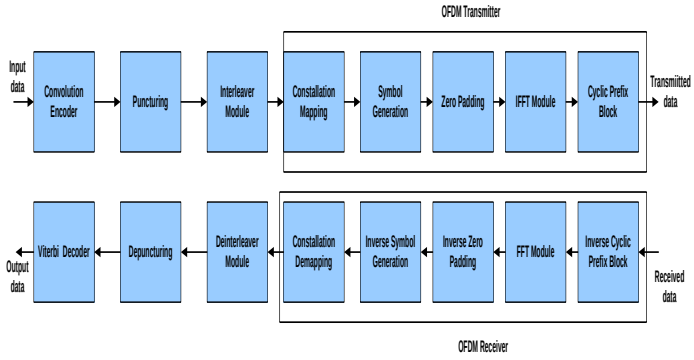

Fig 1. MIMO-OFDM Block Diagram

3.1 TRANSMITTER DESIGN:

The transmitter design block contains mainly the forward error correction (FEC) blocks include convolution encoding, puncturing and interleaving. For this analysis, a coding rate of 1/3 is used for 16-QAM modulation. Next step is interleaving using a matrix interleaver, whose size varies according to the modulation scheme used and system configuration , which follows the OFDM modulation schemes which includes constellation mapping, symbol generator, zero padding, IFFT and Cyclic prefix insertion.

3.1.1 Convovltion Encoder Design:

A convolutional code introduces input bits into the data stream through the use of shift registers. Convolutional codes are defined by three parameters (m, n, k).
Where, m = number of input bits
n = number of output bits
k = Constraint length

The quantity m/n called the code rate is a measure of the efficiency of the code. In this paper presents the convolutional encoder defined for m =1, n = 3 and k = 7.The codification rate R= m/n =1/3 and constraint length k = 7.

3.1.2 Punturing design:

Puncturing is the regular/periodic deletion of parity bits from a convolutional encoder output to increase the rate of the code. Such deletion can reduce the free distance of the code. A concept often used in either or both of the convolutional codes in a concatenated Turbo Coding system. Puncturing allows a single code to be used at different code rates, which may be useful in systems that transmit at different data rates depending on conditions. Design or use of a different code for each data rate might complicate implementation. With turbo codes, it is the interleaver that provides the additional gain and it may be that the overall code sees little difference with puncturing from what might have been achieved using a better constituent high-rate code. Thus, puncturing is often used with turbo codes to simplify the implementation at several rates with the same encoder.

3.1.3 Interleaver design:

Interleaving is used to spread out the errors occurring in bursts like those exhibited in fading channels. There are two classical kinds of interleavers, commonly referred to as block and convolutionalA variation of a block interleaver is a pseudorandom block interleaver, in which data is written in memory in sequential order and read in a pseudorandom order. In a convolutional interleaver, the data is multiplexed into and out of a fixed number of shift registers. The two most commonly used type of block interleavers are Matrix interleaver and Random interleaver. The working of block interleaver is being studied and identifies a certain class of block interleavers to show that which is more optimal with respect to bit error rate for different modulation schemes in orthogonal frequency division multiplexing. The Matrix Interleaver performs block interleaving by filling a matrix with the input symbols row by row and then sending the matrix contents to the output port column by column.

3.1.4 Modulation design

A constellation mapper takes a serial bit stream as its input and segments the stream into N-bit symbols, which are mapped to coordinates in the signal constellation. The coordinates of each point in a 2-d signal constellation represents the baseband in-phase and quadrature (I-Q) components that modulate the orthogonal IF carrier signals.
The modulations taken into account are BPSK, 4-QAM and 16-QAM. In our paper we are using 16-QAM. Depending on the modulation the amount of N bits 16 Implementation of a Transmitter OFDM System in a FPGA changes: 1 bit for BPSK, 2 bits for the 4-QAM and 4 bits for 16-QAM.

3.1.5 IFFT design block:

We have to implement the OFDM transmitter block by block and finally interconnect all of them together to form complete OFDM transmitter.
Inverse Fast Fourier Transform (IFFT) 8- point is used to generate OFDM symbols. IFFT converts input signals from frequency domain to time domain and is used in transmitter to handle this process of conversion.
Initially carrier bank generating a set of subcarriers was necessary for OFDM in conventional or analogue approach. Each subcarrier was modulated with a constellation. So to make system digital, simple, cheap, and efficient IFFT is being used.

3.2 RECEIVER DESIGN:

MIMO receiver model contains mainly: inverse operation of transmitter is done. The output was transformed back to the in-phase and quadrature components by the FFT block. The demodulator block demaps them into symbols then converts them into a serial bit stream. The Deinterleaver block produces reverse operation of interleaver and depuntured and then it is provided as input to the Viterbi Decoder that recovers the binary data that should be the same as original Input signal.

3.2.1 Inverse cyclic prefix design:

Inverse cyclic prefix block performs inverse operation of cyclic prefix. It removes the prefixing of symbols done in the cyclic prefix.

3.2.2 FFT block design:

We have to implement the OFDM receiver block by block and finally interconnect all of them together to form complete OFDM receiver. FFT performs inverse operation of IFFT. It converts signals from time domain to frequency domain and is used in receiver to handle this process of conversion. Because viewing, analyzing, and mathematical manipulations are easy in frequency domain.

3.2.3 Inverse zero padding block:

Inverse Zero padding removes the appending zeros to a signal. It demaps a length M signal to a length N < M signal. Inverse Zero padding in the frequency domain is used extensively in practice to compute heavily interpolated spectra.

3.2.4 Inverse symbol generation block:

The inverse symbol generator decreases the number of bits by deleting the replicating the modulated output and produces the signal.

3.2.5 Demodulation design:

The demodulator block demaps them into symbols then converts them into a serial bit stream. These streams are then combined into a serial data, which is an estimate of the original binary data at the transmitter.

3.2.6 Deinterleaver design:

For the deinterleaver, the delays introduced at each branch are complementary to the interleaver. With this interleaving structure, every symbol incurs a fixed delay through the combination of the interleaver and deinterleaver. For synchronization purposes, the sync bytes and inverted sync bytes must be routed to the first branch of the interleaver, which corresponds to a null delay.

3.2.7 Depunturing design:

If puncturing is employed in the encoder, the decoder will have to "depuncture" the data before decoding. Depuncturing is done by inserting NULL symbols for the punctured symbols. NULL symbols are either '0' or '1'.

3.2.8 Modified viterbi decoder design:

A high level view of the implemented adaptive Viterbi decoder architecture used in our paper. The decoder contains a data path and an associated control path. Like most Viterbi decoder, the data path is split into four parts: the Branch Metric Generators (BMG), Add Compare Select (ACS) units, the survivor memory unit, and path metric storage and control. A BMG unit determines path costs and identifies lowest cost paths. Here the lowest cost path means the path with minimum hamming distance. The survivor memory stores lowest cost bit sequence paths on decisions made by the ACS units, and the path metric array holds per state path metrics. The flow of data in the data path and the storage of results are determined by the control path.

4 SIMULATION RESULTS AND ANALYSIS.

Xilinx Integrated Software Environment (ISE) is used for modeling and synthesizing designs for implementation in a Xilinx field programmable gate array (FPGA).In this project an efficient way to design the orthogonal frequency division multiplexing transmitter for FPGA is to be provided and a special design method is to be used implement the interleaver which is better in terms of speed and occupies lesser area which in turn improves the performance of the orthogonal frequency division multiplexing communication system. Proposed OFDM communication system blocks are implemented based on the following algorithms and tested using Verilog in Xilinx ISE.

The MIMO Transceiver design results are as shown below. Fig 2.1(a) shows the top module of the MIMO Transceiver design, fig 2.1(b) shows the MIMO Transceiver design for simulation results.

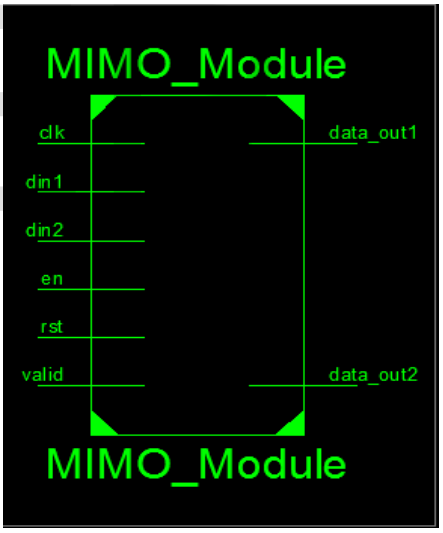

Fig 2.1(a) MIMO Transceiver top module

The simulation results for MIMO Transceiver as shown below. Clock is always toggling, reset initial '1' enable ='1',valid='1' ,data_in1='0', data_in2='0' run few clock cycles, then reset='0' . run few clock cycles. And get the data_out1='0', data_out2='0' and give data_in1='1', data_in2='1'and en='0' few clock cycles then en='1', the outputs data_out1='1' and dta_out2='1'.

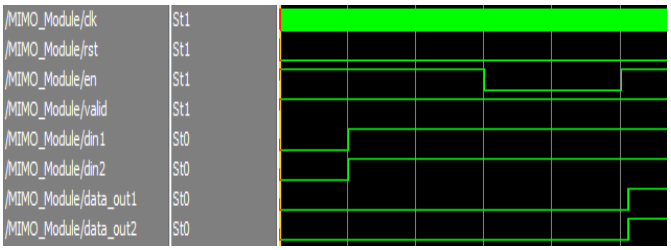

Fig 2.1(b) MIMO Transceiver simulation results

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	14952	301440	4%
Number of Slice LUTs	27603	150720	18%
Number of fully used LUT-FF pairs	10870	31685	34%
Number of bonded IOBs	8	720	1%
Number of BUFG/BUFGCTRLs	12	32	37%
Number of DSP48E1s	36	768	4%

Fig 2.1(c) MIMO Transceiver synthesis results.

The simulation results for transmitter as shown below. Clock is always toggling, reset initial '1', valid='1', data_in='1' run few clock cycles, then reset='0'. run few clock cycles and get the 16-bit data_out values.

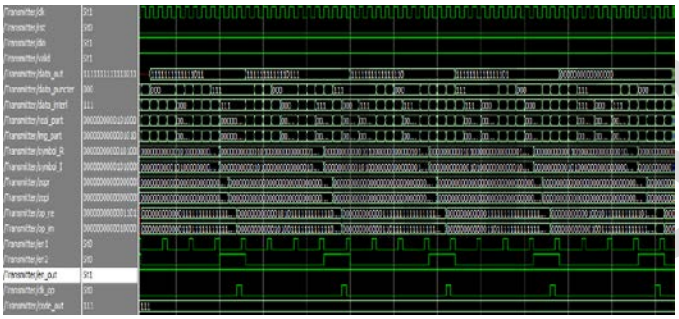

Fig 2.1(d) Transmitter simulation results

The simulation results for receiver as shown below. Clock is always toggling, reset initial '1', valid='1', data_in="1111111111111011" run few clock cycles, then reset='0'. Run few clock cycles and get the 1-bit data_out value.

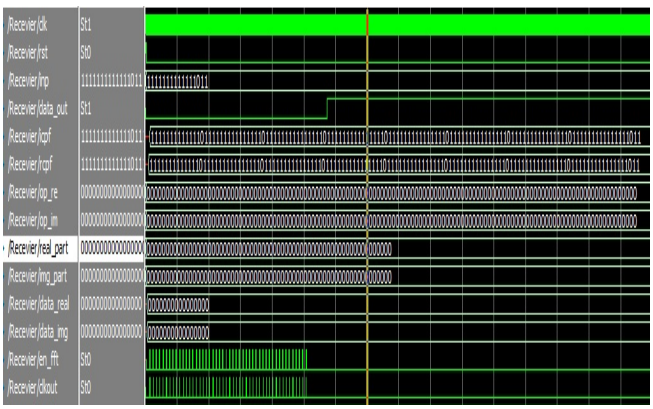

Fig 2.1(e) receiver simulation results

5 Conclusion

An efficient MIMO-OFDM technique is been developed for the transmitting and receiving unit of the OFDM technique with optimized encoding and decoding design for increasing the efficiency of the system by optimizing the area based on FPGA. Simulation study of modulation scheme-16-QAM deployed over OFDM using code rate 1/3 with interleaver (Matrix) is studied. Convolution encoder and modified decoder's resource Utilization is analyzed with respect to OFDM over an AWGN channel. New architecture of the transmitting unit and receiving unit is simulated, implemented on FPGA and tested for the given system.

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